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David L McCombs
Haynes And Boone LLP
901 Main Street
Suite 3100
Dallas, TX 75202-3789

EXAMINER
LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
2189	10

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/672,131	Applicant(s) KITTEN ET AL.	
	Examiner Christopher E. Lee	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-10 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10 and 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 7th of July, 2003. Claims 1 and 8 have been amended; claims 4, 11 and 16 have been canceled; and no claim has been newly added since the Office Action was mailed on 7th of April, 2002. Currently, claims 1-3, 5-10 and 12-15 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. [US 5,675,641 A; hereinafter Watanabe] in view of Waller, Jr. [US 5,268,527; hereinafter Waller].

Referring to claim 1, Watanabe discloses an apparatus (i.e., circuit 200 of Fig. 2) comprising: a first audio (i.e., speaker 221 of Fig. 2) input/output connector (i.e., connection part between speaker and the amplified signal line); at least one second audio input/output connector (i.e., earphone jack 240 of Fig. 2); an audio controller (i.e., controller 250 of Fig. 2); a circuit (i.e., amplifier 222 of Fig. 2) coupling said first audio input/output connector to said audio controller (See speaker circuit 220 in Fig. 2); at least one circuit (i.e., earphone detector 228 of Fig. 2) coupling at least one second audio input/output connector (i.e., earphone jack 240 of Fig. 2) to said audio controller (See speaker circuit 220 in Fig. 2); and a device (i.e., decoupling switch 227 of Fig. 2) electrically decoupling said first audio input/output connector from said circuit coupling said first audio input/output connector to said audio controller when an audio input/output device (i.e., earphone) is coupled to at least one second input/output connector (i.e., earphone jack 240 of Fig. 2; See col. 3, lines 4-43).

Watanabe does not teach a direct-current blocking cap including a filter circuit coupled with an inverting amplifier, wherein said device is coupled between said direct-current blocking cap and a primary audio input/output coupling.

Waller discloses a direct-current blocking cap (i.e., reactance simulation circuit 30 of Fig. 5; See col. 5, lines 36-39) including a filter circuit (i.e., bandpass filter circuit 50 of Fig. 5) coupled with an inverting amplifier (i.e., inverting amplifier 43 of Fig. 5), wherein a device (i.e., level control 20 of Fig. 5) is coupled between said direct-current blocking cap (i.e., reactance simulation circuit) and a primary audio input/output coupling (i.e., input terminal 11 and input buffer 10 of Fig. 5, as combined).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said direct-current blocking cap (i.e., reactance simulation circuit), as disclosed by Waller, in said apparatus, as disclosed by Watanabe, for the advantage of providing a fundamental resonance peak at approximately 85 Hz and also providing a rising high frequency level above 1KHz (See Waller, col. 4, line 68 through col. 5, line 3, and col. 5, lines 26-60).

Referring to claim 5, Watanabe teaches said device comprises a mechanical switch (i.e., decoupling switch 227 of Fig. 2).

Referring to claim 7, Watanabe teaches said second audio input/output connector comprises a jack (i.e., earphone jack 240 of Fig. 2).

4. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe [US 5,675,641 A] in view of Waller [US 5,268,527] as applied to claims 1, 5 and 7 above, and further in view of Fujii et al. [US 6,128,263 A; hereinafter Fujii].

Referring to claim 2, Watanabe, as modified by Waller, discloses all the limitations of the claim 2 except that does not teach said device comprises a transistor.

Fujii discloses a computer motherboard 100 (Fig. 7), wherein a device (i.e., noise removal mechanism; See col. 16, lines 60-62) electrically decoupling (See col. 17, lines 6-9) a first audio input/output

connector (i.e., line input on interface connector 260 in Fig. 7) from a circuit (i.e., receiver 402 of Fig. 7) coupling said first audio input/output connector to an audio controller (i.e., audio controller 37 of Fig. 1) when an audio input/output device (i.e., CPU 220 of CD-ROM drive 200 of Fig. 7) is coupled to at least one second input/output connector (i.e., mute signal on interface connector 260 in Fig. 7) comprises a transistor (i.e., n-channel FET 401 of Fig. 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said device (i.e., noise removal mechanism), as disclosed by Fujii, for said device (i.e., decoupling switch), as disclosed by Watanabe, as modified by Waller, for the advantage of replacing the mechanical contact of said device, which produces an electro-mechanical noise, with the transistor switch (i.e., FET switch), which does not produce said noise. This advantage is well known to one of ordinary skill in the art of electronics circuit design at the time the invention was made. Therefore, the transistor switch (i.e., FET transistor) receives at its gate said second audio input/output detecting signal (i.e., mute signal) from said device (i.e., CPU) during said second audio input/output operation period (i.e., mute period), a high voltage is applied to the gate, and accordingly, the output of said first audio input/output signal (i.e., output driver 232 of Fig. 7; Fujii) goes to the ground level, thus said audio input/output signal to said first audio input/output connector (i.e., unwanted signal) is not output to said first audio input/output device (i.e., speaker) when said second audio input/output device is coupled (i.e., earphone is coupled to an earphone jack). Refer to Fujii, col. 16, lines 13-20.

Referring to claim 3, Watanabe, as modified by Waller and Fujii, teaches said transistor (i.e., n-channel FET switch 401 of Fig. 7; Fujii) is a field effect transistor comprising a drain, a source, and a gate (See Fujii, col. 16, lines 60-67), wherein said drain is coupled to said first audio input/output connector (i.e., line input on interface connector 260 is coupled to the drain of n-channel FET switch 401 in Fig. 7; Fujii), said source is coupled to ground (See Fujii, col. 16, lines 62-64), and said gate is coupled to at least one second audio input/output connector (See Fujii, col. 16, lines 64-67) such that current flows into said

gate when an audio input/output device (i.e., earphone; Watanabe) is coupled to a second audio input/output connector (i.e., earphone jack 240 of Fig. 2; Watanabe) to which said gate is coupled (i.e., a mute signal input by the drive unit is received at the gate of the FET switch anticipates said second audio input/output device detection (i.e., earphone detection signal) input by a detecting device (i.e., earphone detector) is received at the gate of said FET switch).

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe [US 5,675,641 A] in view of Waller [US 5,268,527] as applied to claims 1, 5 and 7 above, and further in view of Fang et al. [US 6,050,854 A; hereinafter Fang].

Referring to claim 6, Watanabe, as modified by Waller, discloses all the limitations of the claim 6 except that does not teach said first audio input/output connector comprises a jack.

Fang discloses an audio connector (i.e., jack; See Fang, col. 1, lines 10-13) includes a shielding for preventing noise (See col. 1, lines 6-8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said audio connector, as disclosed by Fang, in said apparatus for coupling between an audio device (e.g., speaker) to a circuit (e.g., amplifier), as disclosed by Watanabe, as modified by Waller, so as to replace the speaker conveniently in case of being failed, and for the advantage of effectively suppressing EMI from affecting the function of audio, as well (See Fang, col. 1, lines 41-43).

6. Claims 8, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keene [US 5,553,220 A] in view of Watanabe [US 5,675,641 A] and Waller [US 5,268,527].

Referring to claim 8, Keene discloses a computer system (i.e., computer-based multimedia system in Fig. 2), comprising: a processor (i.e., host CPU 111 of Fig. 2); a memory (i.e., audio data buffer 215 of Fig. 2) coupled to said processor (See Fig. 5; i.e., said audio data buffer is coupled to said host CPU); an audio controller (i.e., CODEC audio controller 201 of Fig. 2) coupled to said processor (See Fig. 5; i.e., said audio controller is coupled to said host CPU).

Keene does not expressly disclose a first audio input/output connector coupled to said audio controller; at least one second audio input/output connector coupled to said audio controller; and a device electrically decoupling said first audio input/output connector from a circuit coupling said first audio input/output connector to said audio controller when an audio input/output device is coupled to at least one second input/output connector.

Watanabe teaches a dual mode speaker telephone (Fig. 2), wherein an apparatus (i.e., speaker circuit 220 of Fig. 2) comprising: a first audio (i.e., speaker 221 of Fig. 2) input/output connector (i.e., connection part between speaker and the amplified signal line) coupled to an audio controller (See controller 250 and speaker circuit 220 in Fig. 2); at least one second audio input/output connector (i.e., earphone jack 240 of Fig. 2) coupled to said audio controller (See speaker circuit 220 in Fig. 2); and a device (i.e., decoupling switch 227 of Fig. 2) electrically decoupling said first audio input/output connector from a circuit coupling said first audio input/output connector to said audio controller when an audio input/output device (i.e., earphone) is coupled to at least one second input/output connector (i.e., earphone jack 240 of Fig. 2; See col. 3, lines 4-43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said speaker circuit, as disclosed by Watanabe, in said apparatus, as disclosed by Keene, for the advantage of operating said audio device (i.e., microphone and speaker/headphone) capable of switching between half-duplex and full-duplex modes of operation (See Watanabe, col. 1, lines 52-62).

Keene, as modified by Watanabe, does not teach a direct-current blocking cap including a filter circuit coupled with an inverting amplifier, wherein said device is coupled between said direct-current blocking cap and a primary audio input/output coupling.

Waller discloses a direct-current blocking cap (i.e., reactance simulation circuit 30 of Fig. 5; See col. 5, lines 36-39) including a filter circuit (i.e., bandpass filter circuit 50 of Fig. 5) coupled with an inverting

amplifier (i.e., inverting amplifier 43 of Fig. 5), wherein a device (i.e., level control 20 of Fig. 5) is coupled between said direct-current blocking cap (i.e., reactance simulation circuit) and a primary audio input/output coupling (i.e., input terminal 11 and input buffer 10 of Fig. 5, as combined). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said direct-current blocking cap (i.e., reactance simulation circuit), as disclosed by Waller, in said apparatus, as disclosed by Keene, as modified by Watanabe, for the advantage of providing a fundamental resonance peak at approximately 85 Hz and also providing a rising high frequency level above 1KHz (See Waller, col. 4, line 68 through col. 5, line 3, and col. 5, lines 26-60).

Referring to claim 12, Watanabe teaches said device is a mechanical switch (i.e., decoupling switch 227 of Fig. 2).

Referring to claim 15, Watanabe teaches said second audio input/output connector comprises a jack (i.e., earphone jack 240 of Fig. 2).

7. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keene [US 5,553,220 A] in view of Watanabe [US 5,675,641 A] and Waller [US 5,268,527] as applied to claims 8, 12 and 15 above, and further in view of Fujii [US 6,128,263 A].

Referring to claim 9, Keene, as modified by Watanabe and Waller, discloses all the limitations of the claim 9 except that does not teach said device comprises a transistor.
Fujii discloses a computer motherboard 100 (Fig. 7), wherein a device (i.e., noise removal mechanism; See col. 16, lines 60-62) electrically decoupling (See col. 17, lines 6-9) a first audio input/output connector (i.e., line input on interface connector 260 in Fig. 7) from a circuit (i.e., receiver 402 of Fig. 7) coupling said first audio input/output connector to an audio controller (i.e., audio controller 37 of Fig. 1) when an audio input/output device (i.e., CPU 220 of CD-ROM drive 200 of Fig. 7) is coupled to at least one second input/output connector (i.e., mute signal on interface connector 260 in Fig. 7) comprises a transistor (i.e., n-channel FET 401 of Fig. 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said device (i.e., noise removal mechanism), as disclosed by Fujii, for said device (i.e., decoupling switch), as disclosed by Keene, as modified by Watanabe and Waller, for the advantage of replacing the mechanical contact of said device, which produces an electro-mechanical noise, with the transistor switch (i.e., FET switch), which does not produce said noise. This advantage is well known to one of ordinary skill in the art of electronics circuit design at the time the invention was made. Therefore, the transistor switch (i.e., FET transistor) receives at its gate said second audio input/output detecting signal (i.e., mute signal) from said device (i.e., CPU) during said second audio input/output operation period (i.e., mute period), a high voltage is applied to the gate, and accordingly, the output of said first audio input/output signal (i.e., output driver 232 of Fig. 7; Fujii) goes to the ground level, thus said audio input/output signal to said first audio input/output connector (i.e., unwanted signal) is not output to said first audio input/output device (i.e., speaker) when said second audio input/output device is coupled (i.e., earphone is coupled to an earphone jack). Refer to Fujii, col. 16, lines 13-20.

Referring to claim 10, Keene, as modified by Watanabe, Waller and Fujii, teaches said transistor (i.e., n-channel FET switch 401 of Fig. 7; Fujii) is a field effect transistor comprising a drain, a source, and a gate (See Fujii, col. 16, lines 60-67), wherein said drain is coupled to said first audio input/output connector (i.e., line input on interface connector 260 is coupled to the drain of n-channel FET switch 401 in Fig. 7; Fujii), said source is coupled to ground (See Fujii, col. 16, lines 62-64), and said gate is coupled to at least one second audio input/output connector (See Fujii, col. 16, lines 64-67) such that current flows into said gate when an audio input/output device (i.e., earphone; Watanabe) is coupled to a second audio input/output connector (i.e., earphone jack 240 of Fig. 2; Watanabe) to which said gate is coupled (i.e., a mute signal input by the drive unit is received at the gate of the FET switch anticipates said second audio input/output device detection (i.e., earphone detection signal) input by a detecting device (i.e., earphone detector) is received at the gate of said FET switch).

8. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keene [US 5,553,220 A] in view of Watanabe [US 5,675,641 A] and Waller [US 5,268,527] as applied to claims 8, 12 and 15 above, and further in view of Fang [US 6,050,854 A].

Referring to claim 13, Keene, as modified by Watanabe and Waller, discloses all the limitations of the claim 13 except that does not teach said first audio input/output connector is a jack.

Fang discloses an audio connector (i.e., jack; See Fang, col. 1, lines 10-13) includes a shielding for preventing noise (See col. 1, lines 6-8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said audio connector, as disclosed by Fang, in said apparatus for coupling between an audio device (e.g., speaker) to a circuit (e.g., amplifier), as disclosed by Keene, as modified by Watanabe and Waller, so as to replace the speaker conveniently in case of being failed, and for the advantage of effectively suppressing EMI from affecting the function of audio, as well (See Fang, col. 1, lines 41-43).

Referring to claim 14, Watanabe teaches said second audio input/output connector comprises a jack (i.e., earphone jack 240 of Fig. 2).

Response to Arguments

9. *Applicants' arguments* with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

10. *In response to applicants' argument* that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

11. *In response to applicants' argument* that the Examiner's conclusion of obviousness for the *35 USC §103(a)* rejection fails to establish a *prima facie* case of obviousness, the Examiner respectfully disagrees. In contrary to the Applicant's statement, all the rejections under *35 USC §103(a)* in the prior and the instant Office Action established a *prima facie* case of obviousness meeting the three basic criteria of the M.P.E.P. 2143.03 (8th ed. 2001). See the Office Action mailed on 7th of April, 2003. Furthermore, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner has clearly pointed out rationale for appropriate combination of the references. Thus, the Applicants' argument on this point is not persuasive.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to filtering,

Yokoyama et al. [US 4,303,889] disclose filter circuit.

Muljadi et al. [US 5,747,967 A] disclose apparatus and method for maximizing power delivered by a photovoltaic array.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

cel/ CEL
July 17, 2003

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100